

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Craig T. Salling, et al.

Art Unit: 2813

Division of Serial No.: 09/975,107

Examiner: David L. Hogans

Filed: Herewith

Docket: TI-32206.1

For: Method to Increase Substrate Potential in MOS Transistors Used in ESD Protection Circuits

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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hereby certify that this paper is being deposited with the U.S.
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VA 22313-1450.

Karen Vertz

7-29-03

Date

PRELIMINARY AMENDMENT

Dear Sir:

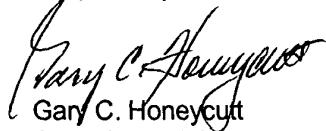
Prior to the examination of the above-identified application, please amend as follows:

IN THE CLAIMS:

Please cancel Claims 1-11.

Should the Examiner have any further comments or suggestions, it is respectfully requested
that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Respectfully submitted,


Gary C. Honeycutt
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Attorney for Applicants

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